

Teaching Diary

2018-19

Radar Systems

Digital Signal Processors & Architecture

Sl. No.	DATE	PERIOD	TOPICS TAUGHT	REMARKS
1.	24/12/18	3 rd	Introduction to digital signal processing.	
2.				
2.	27/12/18	2 nd	The sampling process	
	27/12/18	2 nd	Discrete time sequences.	
3.	29/12/18	1 st , 3 rd , 4 th	DFT.	
4.	05/01/19	1 st , 3 rd	FFT	
5.	08/01/19	2 nd	LT system.	
6.	10/01/19	1 st	Digital filters.	
7.	17/01/19	1 st	Decimation & interpolation.	
8.	19/01/19	1 st	No. formats for dsp signals and coefficients.	
9.	22/01/19	2 nd	Dynamic range & precision.	
	22/01/19	2 nd .	Sources of errors in dsp systems	
10.	31/01/19	1 st	A/D conversion errors.	
11.	02/02/19	1 st	D/A conversion errors.	
12.	04/02/19	3 rd	Dsp computational errors.	
	04/02/19	3 rd	Compensating filter.	
13.	05/02/19	2 nd	Architecture for programmable dsp devices.	
14.	07/02/19	1 st	Basic architectural features	
15.	07/02/19	1 st	Dsp computational Building blocks.	
	09/02/19	1 st		
15.	11/02/19	3 rd	Bus architecture & memory	
	11/02/19	3 rd	Data addressing capabilities.	
16.	12/02/19	2 nd	address generation unit.	
	12/02/19	2 nd	programmability &	
	12/02/19	2 nd	Program execution	
	12/02/19	2 nd	Speed issues.	
17.	14/02/19	1 st	features for external interfacing.	
	14/02/19	1 st	programmable digital signal processors.	
			commercial digital signal	

[Signature]
Lecturer

[Signature]
H.O.D.

[Signature]
Principal



Sl. No.	DATE	PERIOD	TOPICS TAUGHT	REMARKS
18	21/2/19 23/02/19	1 st	Processing devices - data addressing model of TMS320C54XX processors	
19	23/02/19	1 st	memory space of TMS320C54XX processors.	
20	25/02/19	3 rd	Program Control.	
21	26/02/19	2 nd	TMS320C54XX instructions & programming.	
	28/02/19	1 st	onchip peripherals.	
22	02/03/19	2 nd	Interrupts of TMS320C54XX processors.	
	02/03/19	1 st	pipeline operation of TMS320C54 processor.	
23	05/03/19	2 nd	analog devices Inter-facing memory & I/O peripherals. to programmable dsp devices.	
24	07/03/19	1 st	memory space organization External bus inter-facing signals	
25	09/03/19	1 st	memory Inter-face I/O interface	
26	11/03/19	3 rd	programmed I/O interrupts.	
27	12/03/19	2 nd	Block direct memory access.	
28	14/03/19	1 st	Analog devices family of dsp devices.	
29	16/3/19	1 st	ALU and mac block diagram.	
30	18/3/19	3 rd	Shifter instruction.	
31	19/3/19	2 nd	Basic architecture of A DSP2100.	
32	23/3/19	1 st	higher performance processor.	
33	25/3/19 - 27/3/19	3 rd , 4 th	A DSP - 2181.	
34	28/3/19 - 29/3/19	1 st , 1 st	Introduction to black pin processor.	
35	1/4/19 - 4/4/19	3 rd , 2 nd , 1 st	Introduction to micro signal architecture.	
36	8/4/19 - 9/4/19	3 rd 2 nd		

[Signature]
Lecturer

[Signature]
H.O.D.

[Signature]
Principal



